HIGH PERFORMANCE COMPUTER ARCHITECTURE midterm exam 28-06-2007 **MATRIC.NO.**_____

(former CALCOLATORI ELETTRONICI 2) **SURNAME**_____

FIRST NAME_____

1) (34/40) Consider the following snippet of code running on 4-ways out-of-order superscalar processor. Initially, R1=0x1000, R3=0x3000, R7=0x0003 and the other registers contain zero.

```
lab1:   LW   R2,0(R1)
        LW   R4,0(R3)
        ADD  R5,R5,R2
        ADD  R5,R5,R4
        MUL  R5,R5,R5
        SW   R5,0(R1)
        SW   R5,0(R3)
        ADDI R1,R1,4
        ADDI R3,R3,4
        ADDI R7,R7,-1
        BNE  R7,R0,lab1
```

Working hypothesis:
* the fetch, decode and commit stages are 4 instructions wide
* the instruction window has 16 slots
* we have 24 physical registers in the free pool
* the reorder buffer has unlimited size
* the integer multiplier has 4 stages
* the load/store queues have 3 slots each and a common effective-address calculation unit
* there are 4 ALUs for arithmetic and logic operations and for branching
* an ALU performs its operation in the same cycle when the operation is issued
* reads require 1 clock cycle (after the addressing phase)
* the register file has 4 input- and 4 output-ports
* there are 9 logical registers (including R0 which is hardwired to 0)
* the store operation leaves the issue stage as it is inserted in the store queue

In order to calculate the total cycles needed to execute 3 iterations of the above loop on such machine, complete the following chart until the end of the third iteration of the code fragment above, including the renamed stream the precise evolution of the free pool of the physical registers (the register map), the Instruction Window, the Reorder Buffer (ROB) and the Load Queue (LQ) and Store Queue (SQ).

Iter.	Instruction	F-Fetch (clock)	D-Decode (clock)	P-disPatch (clock)	I-Issue (clock)	X-eXecute (clock)	W-Write-back (clock)	C-Commit (clock)	Renamed Stream	Instruction Window Pi Pj Pk I Qj Qk	Reorder Buffer Ri Pi,old Cplt	Load Queue	Store Queue
1	**LW R2,0(R1)**	0							P2,0(P1)	P2 P1 - 0 0 0	R2 - -		
...	...												
...	...												

2) (6/40) Explain the difference between Processor Consistency and Weak Ordering by motivating the difference with a personal reasoning.