COMPITO di ARCHITETTURA DEI CALCOLATORI del 01-03-2018 **MATRICOLA**_____

DA RESTITUIRE INSIEME AGLI ELABORATI e A TUTTI I FOGLI
→ NON USARE FOGLI NON TIMBRATI
→ ANDARE IN BAGNO PRIMA DELL'INIZIO DELLA PROVA
→ NO FOGLI PERSONALI, NO TELEFONI, SMARTPHONE, ETC

COGNOME_____

NOME_____

SVOLGIMENTO DELLA PROVA (selezionare una delle seguenti 4 opzioni):
☐ PER GLI STUDENTI DI "ARCHITETTURA DEI CALCOLATORI – A.A. 2015/16, 16/17, 17/18": es. N.1+2+3+7.

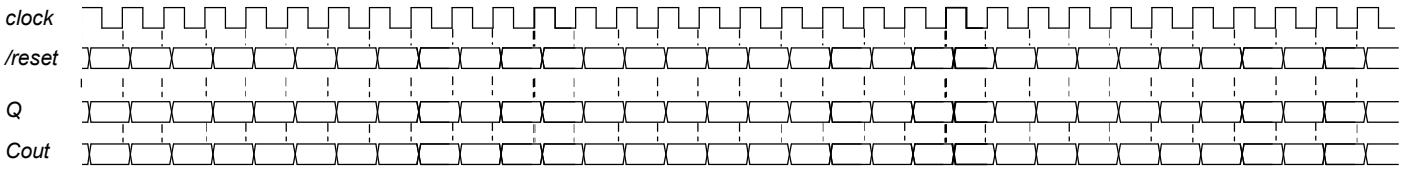
NOTA: per l'esercizio 7 dovranno essere consegnati DUE files: il file del programma VERILOG e il file relativo all'output (screenshot o copy/paste)

1) [18/38] Trovare il codice assembly MIPS corrispondente al seguente programma **(usando solo e unicamente istruzioni della tabella sottostante e rispettando le convenzioni di utilizzazione dei registri dell'assembly MIPS** riportate qua sotto per riferimento).

```
double power(double base, double index) {
    double count = index, result = 1;
    for(count=index; count>=1; count--) {
        result = result*base;
    }
    return result;
}

double differenceOf(double n,double mid) {
    if (n > (power(mid, 3)))
        return (n-power(mid, 3));
    else
        return ((power(mid, 3) - n));
}

double cuberoot(double n) {
    double low=0, high=n, e = 0.0000001, diff;
    double mid = (low+high)/2;

returnHere:
    mid = (low+high)/2;
    diff = differenceOf(n, mid);
    if(diff <= e) {
        return mid;
    } else {
        if((power(mid, 3)) > n) {
            high = mid;
            goto returnHere;
        } else {
            low = mid;
            goto returnHere;
        }
    }
}

int main() {
    double n;
    print_string("Inserisci un nunero: ");
    read_double(&n);
    print_string("La radice cubica e':");
    print_double(cuberoot(n));
    print_string("\n");
    exit(0);
}
```

2) [8/38] Si consideri una cache di dimensione 96B e a 3 vie di tipo write-back/write-non-allocate. La dimensione del blocco e' 8 byte, il tempo di accesso alla cache e' 4 ns e la penalita' in caso di miss e' pari a 40 ns, la politica di rimpiazzamento e' LRU. Il processore effettua i seguenti accessi in cache, ad indirizzi al byte: 355, 373, 315, 319, 322, 347, 318, 349, 334, 348, 377, 319, 283, 243, 391, 344, 370, 345, 61, 394. Tali accessi sono alternativamente letture e scritture. Per la sequenza data, ricavare il tempo medio di accesso alla cache, riportare i tag contenuti in cache al termine, i bit di modifica (se presenti) e la lista dei blocchi (ovvero il loro indirizzo) via via eliminati durante il rimpiazzamento ed inoltre in corrispondenza di quale riferimento il blocco e' eliminato.

3) [4/38] Rappresentare il numero 123/11 in IEEE-754 singola precisione con arrotondamento al numero piu' vicino e in caso di equidistanza arrotondare al valore pari (round to nearest, ties to even).
4) Non assegnato
5) Non assegnato
6) Non assegnato
7) [8/38] **Realizzare** in Verilog (per studenti 2014 e anni precedenti --> v.nota finale) sia un parallel carry counter a 4-bit che il relativo testbench: il clock ha un periodo di 10ns; il segnale _reset e' attivo basso: resta alto per 5ns, basso per 20ns, e poi ritorna alto per 600ns. Il contatore inizia il conteggio producendo sull'uscita Q il valore binario 0000 quando il segnale di /reset e'attivato, appena disattivato il /reset il conteggio prosegue. Assumere inoltre che le porte AND abbiano un ritardo di 1ns. **Tracciare il diagramma di temporizzazione** come verifica della correttezza dell'unità riportando i segnali clock, /reset, uscita Q e Cout (carry in uscita al contotare) per la durata complessiva (625ns). Nota: si può svolgere l'esercizio su carta oppure con ausilio del simulatore salvando una copia dell'output (diagramma temporale) e del programma Verilog su USB-drive del docente. (Per studenti 2014 e anni precedenti descrivere il comportamento di questa rete e disegnare líntero diagramma di temporizzazione, come sopra specificato). Opzionalmente: discutere che differenza c'e' su Cout rispetto allo stesso contatore ma con serial-carry.



COMPITO di ARCHITETTURA DEI CALCOLATORI del 01-03-2018

Instructions

Opcode+Funct (hexadecimal)	Instruction	Example	Meaning	Comments
00+20/00+21	**add**	`add/addu $1,$2,$3`	$1 = $2 + $3	(signed/unsigned) 3 operands; exception possible
00+22/00+23	**subtract**	`sub/subu $1,$2,$3`	$1 = $2 - $3	(signed/unsigned) 3 operands; exception possible
08/09	**add immediate**	`addi/addiu $1,$2,100`	$1 = $2 + 100	(signed/unsigned) + constant ; exception possible
00+18/00+19	**multiplication**	`mult/multu $1, $2`	Hi,Lo= $1 x $2	(signed/unsigned) 64-bit Product ; result in Hi,Lo
00+1A/00+1B	**division**	`div/divu $1, $2`	Hi= $1 % $2, Lo = $1 / $2	(signed/unsigned) division
00+10/00+12	**move from Hi / move from Lo**	`mfhi/mflo $1`	$1 = Hi ($1 = Lo)	Create copy of Hi (Create a copy of Lo)
00+2A/00+2B	**set on less than**	`slt/sltu $1,$2,$3`	if ($2 < $3) $1 = 1; else $1 = 0	(signed/unsigned) compare $2 and $3 (less than)
0A/0B	**set on less than immediate**	`slti/sltiu $1,$2,100`	if ($2 < 100) $1 = 1; else $1 = 0	(signed/unsigned) compare $2 and constant (less than)
00+24/25/26/27	**and / or / xor / nor**	`and/or/xor/nor $1,$2,$3`	$1=$2&$3 / $2|$3 / $2^$3 / !($2|$3)	3 register operands; Logical AND/OR/XOR/NOR
0C/0D/0E	**and /or / xor immediate**	`andi/ori/xori $1,$2,100`	$1 = $2 & 100 / $2 | 100 / $2 ^100	Logical AND/OR/XOR register, constant
00+00	**shift left logical**	`sll $1,$2,10`	$1 = $2 << 10	Shift left by constant
00+02/00+03	**shift right (l=logical,a=arithmetic)**	`srl/sra $1,$2,10`	$1 = $2 >> 10	Shift right by constant (for arithmetic: sign is preserved)
23/20	**load word / load byte**	`lw/lb $1,100($2)`	$1 = Memory[$2+100]	Data from memory to register
24	**load byte unsigned**	`lbu $1,100($2)`	$1 = Memory[$2+100]	Data from mem. To reg.; no sign extension
2B/28	**store word / store byte**	`sw/sb $1,100($2)`	Memory[$2+100] = $1	Data from register to memory
0F	**load upper immediate**	`lui $1,0x1234`	$1=0x1234'0000	load most significant 16 bits
PSEUDOINSTRUCTION	**load address**	`la $1,var`	$1 = &var	Load address of var (lui $1,H16(&var);ori $1, L16(&var)) H16/L16=high/low 16 bits of &var
02	**jump**	`j 10000`	go to 10000	Jump to target address
00+08	**jump register**	`jr $31`	go to $31	For switch, procedure return
03	**jump and link**	`jal 10000`	$31 = PC + 4;go to 10000	For procedure call
04	**branch on equal**	`beq $1,$2,100`	if ($1 = = $2) go to PC+4+100	Equal test; PC relative branch
05	**branch on not equal**	`bne $1,$2,100`	if ($1 != $2) go to PC+4+100	Not equal test; PC relative
00+0C	**syscall**	`syscall`	call OS service $v0	See table of system calls below
10+10,rs=10	**rfe**	`rfe`	shift right (k,e) bits in STATUS reg	Exit Kernel Mode, Enable Interrupts
PSEUDOINSTRUCTION	**branch unconditional**	`b 100`	go to PC+4+100	PC relative branch (e.g., beq $0,$0,100)
PSEUDOINSTRUCTION	**no operation**	`nop`	do nothing	Do nothing (e.g. sll $0,$0,0)
30	**load-linked**	`ll $1,100($2)`	$1=Memory[$2+100]	Read and start to monitor the given memory location
38	**store-conditional**	`sc $1,100($2)`	Memory[$2+100]=$1 or →	return 0 if a coherence action happens since the previous ll ($1 must be different from 0)
11+00 fmt=10/11	**add.s / add.d**	`add.x $f0,$f2,$f4`	$f0=$f2+$f4	Single and double precision add
11+01 fmt=10/11	**sub.s / sub.d**	`sub.x $f0,$f2,$f4`	$f0=$f2-$f4	Single and double precision subtraction
11+02 fmt=10/11	**mul.s / mul.d**	`mul.x $f0,$f2,$f4`	$f0=$f2*$f4	Single and double precision multiplication
11+03 fmt=10/11	**div.s / div.d**	`div.x $f0,$f2,$f4`	$f0=$f2/$f4	Single and double precision division
11+05 fmt=10/11	**abs.s / abs.d**	`abs.x $f0,$f2`	$f0=ABS($f2)	Single and double precision absolute value
11+06 fmt=10/11	**mov.s / mov.d**	`mov.x $f0,$f2`	$f0←$f2	Single and double precision move
11+07 fmt=10/11	**neg.s / neg.d**	`neg.x $f0,$f2`	$f0= – ($f2)	Single and double precision opposite value
11+3C(31,32,3D,3E,3F) fmt=10/11	**c.lt.s / c.lt.d (ne,eq,gt,le,ge)**	`c.lt.x $f0,$f2`	Temp=($f0<$f2)	Single and double: compare $f0 and $f2 <,=,!=,>,<=>=
11+00 fmt=4/0	**move to/from coprocessor 1**	`mtc1/mfc1 $1,$f2`	$f2=$1 / $1=$f2	Move $1 to/from C1reg. $f2 (no conversion)
10+00 fmt=4/0	**move to/from coprocessor 0**	`mtc0/mfc0 $1,$2`	$c2=$1 / $1=$c2	Move $1 to/from C0 reg. $f2 (no conversion)
11+00 fmt=6/2	**move to/from control reg of cop.1**	`ctc1/cfc1 $1,$cf2`	$cf2=$1 / $1=$cf2	Move $1 to/from C1-CONTROL register
11 fmt=8,ft=1/0	**branch on true/false**	`bc1t/bc1f label`	If (Temp = = true/false) go to label	Temp is 'Condition-Code'
31/39	**load/store floating point (32bit)**	`lwc1/swc1 $f0,0($1)`	$f0←Memory[$1] / Memory[$1]←$f0	Data from FP (C1) register to memory
11+21,fmt=10/11+22,fmt=11	**convert from/to single to/from double**	`cvt.d.s/cvt s.d $f0,$f2`	$f0=(double)$f2/$f0=(single)$f2	Type conversion
11+24,fmt=11/11+20	**convert from/to single to/from integer**	`cvt.w.s/cvt s.w $f1,$f0`	$f1=(int)$f0 / $f0=(single)$f2	Type conversion

Register Usage

Name	Reg. Num.	Usage
$zero	0	The constant value 0
$s0-$s7	16-23	Saved
$t0-$t9	8-15,24-25	Temporaires
$a0-$a3	4-7	Arguments

Name	Reg.Num.	Usage
$v0-$v1	2-3	Results
$fp, $sp	30,29	frame pointer, stack pointer
$ra, $gp	31,28	return address, global pointer
$k0-$k1	26,27	Kernel usage

Reg. Num.	Usage
$f0, $f2	Return values
$f12,$f14	Function arguments
$f20,$f22,$f24,$f26,$f28,$f30	Saved registers
$f4,$f6,$f8,$f10,$f16,$f18	Temporaries registers

System calls

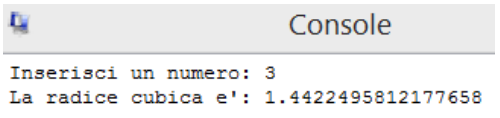
Service Name	Service Num. ($v0)	INPUT Arguments	OUTPUT Arguments
print_int	1	$a0=integer to print	---
print_float	2	$f12=float to print	---
print_double	3	($f12,$f13)=double to print	---
print_string	4	$a0=address of ASCIIZ string to print	---
read_int	5	---	$v0=integer
read_float	6	---	$f0=float
read_double	7	---	$f0-f1=double
read_string	8	$a0=address of input buffer, $a1=max characters to read	---
sbrk	9	$a0=Number of bytes to be allocated	$v0=pointer to the allocated memory
exit	10	---	---

COMPITO di ARCHITETTURA DEI CALCOLATORI del 01-03-2018

SOLUZIONE

ESERCIZIO 1

```
.data
e:    .double 0.0000001
uno:  .double 1.0
due:  .double 2.0
tre:  .double 3.0
msg1: .asciiz "Inserisci un numero: "
msg2: .asciiz "La radice cubica e': "
new1: .asciiz "\n"

.text
.globl main

main:
   #________CALL FRAME___________
   # saved variables: (f20,f21)  8B
   addi    $sp, $sp, -8
   swc1    $f20, 0($sp)
   swc1    $f21, 4($sp)

   la       $a0, msg1
   addi   $v0, $0, 4  #print_string
   syscall

   addi   $v0, $0, 7  #read_double
   syscall
   mov.d   $f20,$f0    #salvo f0

   la       $a0, msg2
   addi   $v0, $0, 4  #print_string
   syscall

   mov.d   $f12,$f20
   jal      cuberoot

   mov.d   $f12, $f0
   addi   $v0, $0, 3  #print double
   syscall

   la $a0, new1
   addi   $v0, $0, 4  #print_string
   syscall

   lwc1     $f20, 0($sp)
   lwc1   $f21, 4($sp)
   addi    $sp, $sp, 8
   addi   $v0, $0, 10 #exit
   syscall

power:
   #________NO CALL FRAME___________
   # base in f12, index in f14
   # count in f4, result in f0
   mov.d   $f4, $f14   #count=index
   la      $t0,uno
   lwc1   $f0,0($t0)
   lwc1   $f1,4($t0)
   mov.d   $f4, $f14   #count=index
   mov.d   $f8,$f0     # 1.0
for1:
   c.le.d  $f8,$f4     # 1.0<=count
   bc1f   finefor1
   mul.d   $f0,$f0,$f12#result*=base
   sub.d   $f4,$f4,$f8 #count--
   j      for1
finefor1:
   jr      $ra

differenceof:
   #________CALL FRAME___________
   # saved variables: fp,ra   8B
   # saved variables: (f12,f13)8B
   # saved variables: (f14,f15)8B
   #____________________Totale 24B
   # n in f12, mid in f14
   addi    $sp,$sp,-24
   sw      $fp,  0($sp)
   add     $fp, $sp, $0
   sw      $ra,  4($sp)
   swc1    $f20, 8($fp)
   swc1    $f21,12($fp)
   swc1    $f22,16($fp)
   swc1    $f23,20($fp)

   mov.d   $f20,$f12  # salvo n
   mov.d   $f22,$f14  # salvo mid

   mov.d    $f12,$f22  #mid
   la      $t0,tre
   lwc1   $f14,0($t0)
   lwc1   $f15,4($t0)#carico 3.0
   jal      power
   c.le.d  $f20,$f0   #n<=?power
   bc1t    else1
   mov.d    $f12,$f22  #mid
   la      $t0,tre
   lwc1   $f14,0($t0)
   lwc1   $f15,4($t0)#carico 3.0
   jal      power
   sub.d   $f0,$f20,$f0 #n-power
   j       retdof
else1:
   mov.d    $f12,$f22  #mid
   la      $t0,tre
   lwc1   $f14,0($t0)
   lwc1   $f15,4($t0)#carico 3.0
   jal      power
   sub.d   $f0,$f0,$f20 #power-n

retdof:
   lwc1    $f23,20($fp)
   lwc1    $f22,16($fp)
   lwc1    $f21,12($fp)
   lwc1    $f20, 8($fp)
   lw      $ra,  4($sp)
   lw      $fp,  0($sp)
   addi    $sp,$sp,24
   jr      $ra

cuberoot:
   #________CALL FRAME___________
   # saved variables: fp,ra   8B
   # saved variables: (f12,f13)8B
   #____________________Totale 16B
   # n in f12, mid in f14
   addi    $sp,$sp,-16
   sw      $fp,  0($sp)
   add     $fp, $sp, $0
   sw      $ra,  4($sp)
   swc1    $f20, 8($fp)
   swc1    $f21,12($fp)

   mov.d   $f20,$f12   # salvo n
   mtc1   $0, $f22
   mtc1   $0, $f23    # low=0.0
   mov.d   $f24,$f20   # high=n
   la      $t0,e
   lwc1   $f26,0($t0)
   lwc1   $f27,4($t0) # f26=e
   la      $t0,due
   lwc1   $f30,0($t0)
   lwc1   $f31,4($t0) # f30=2.0
   add.d   $f28,$f22,$f24 # low+high
   div.d   $f28,$f28,$f30 # /2

returnhere:
   add.d   $f28,$f22,$f24 # low+high
   div.d   $f28,$f28,$f30 # /2
   mov.d   $f12,$f20   # n
   mov.d   $f14,$f28   # mid
   jal      differenceof
   c.le.d  $f0,$f26  #diff<=?e
   bc1f   else2
   mov.d   $f0,$f28
   j      retcr
else2:
   mov.d   $f12,$f28  # mid
   la      $t0,tre
   lwc1   $f14,0($t0)
   lwc1   $f15,4($t0) # 3.0
   jal      power
   c.le.d  $f0,$f20  #power<=? n
   bc1t    else3
   mov.d   $f24,$f28 #high=mid
   j       returnhere
else3:
   mov.d    $f22,$f28 #low=mid
   jal      returnhere

retcr:
   lwc1    $f21,12($fp)
   lwc1    $f20, 8($fp)
   lw      $ra,  4($sp)
   lw      $fp,  0($sp)
   addi    $sp,$sp,16
   jr      $ra
```



ESERCIZIO 2

A = 3, B = 8, C = 96, RP = LRU, Thit = 4, Tpen = 40

```
=== T    X   XM  XT  XS  XB  H [SET]:USAGE [SET]:MODIF  [SET]:TAG
=== R  355   44  11   0   3  0 [0]:2,0,0 [0]:0,0,0  [0]:11,-,-
=== W  373   46  11   2   5  0 [2]:2,0,0 [2]:0,0,0  [2]:11,-,-
=== R  315   39   9   3   3  0 [3]:2,0,0 [3]:0,0,0  [3]:9,-,-
=== W  319   39   9   3   7  1 [3]:2,0,0 [3]:1,0,0  [3]:9,-,-
=== R  322   40  10   0   2  0 [0]:1,2,0 [0]:0,0,0  [0]:11,10,-
=== W  347   43  10   3   3  0 [3]:1,2,0 [3]:1,0,0  [3]:9,10,-
=== R  318   39   9   3   6  1 [3]:2,1,0 [3]:1,0,0  [3]:9,10,-
=== W  349   43  10   3   5  1 [3]:1,2,0 [3]:1,1,0  [3]:9,10,-
=== R  334   41  10   1   6  0 [1]:2,0,0 [1]:0,0,0  [1]:10,-,-
=== W  348   43  10   3   4  1 [3]:1,2,0 [3]:1,1,0  [3]:9,10,-
=== R  377   47  11   3   1  0 [3]:0,1,2 [3]:1,1,0  [3]:9,10,11
=== W  319   39   9   3   7  1 [3]:2,0,1 [3]:1,1,0  [3]:9,10,11
=== R  283   35   8   3   3  0 [3]:1,2,0 [3]:1,0,0  [3]:9,8,11 (out: XM=43 XT=10 XS=3 )
=== W  243   30   7   2   3  0 [2]:1,2,0 [2]:0,0,0  [2]:11,7,-
=== R  391   48  12   0   7  0 [0]:0,1,2 [0]:0,0,0  [0]:11,10,12
=== W  344   43  10   3   0  0 [3]:0,1,2 [3]:1,0,0  [3]:9,8,10 (out: XM=47 XT=11 XS=3 )
=== R  370   46  11   2   2  1 [2]:2,1,0 [2]:0,0,0  [2]:11,7,-
=== W  345   43  10   3   1  1 [3]:0,1,2 [3]:1,0,1  [3]:9,8,10
=== R   61    7   1   3   5  0 [3]:2,0,1 [3]:0,0,1  [3]:1,8,10 (out: XM=39 XT=9  XS=3 )
=== W  394   49  12   1   2  0 [1]:1,2,0 [1]:0,0,0  [1]:10,12,-
-------------------------------------
P1 Nmiss=13   Nhit=7  Nref=20  mrate=0.650000   AMAT=30
```

COMPITO di ARCHITETTURA DEI CALCOLATORI del 01-03-2018

SOLUZIONE

ESERCIZIO 3

Normalizzando 123/11 si ottiene: 123/88*2^3 ovvero m=123/88, e=3. Ricaviamo quindi S,M,E.

L' "uno" iniziale non viene rappresentato nel formato IEEE-754. Essendo m = 123/88=1.397727 si ha:

M = m-1= $\overline{0}$.397727

Successivamente si puo' ricavare la rappresentazione binaria di M con 23 bit moltiplicando per 2 e ricavando via via la n-esima cifra piu' significativa:

0.397$\overline{727}$ *2 = 0.795$\overline{4}$ → **0**, 0.795$\overline{4}$ * 2 = 1.5$\overline{90}$ → **1**, 0.5$\overline{90}$*2= 1.$\overline{18}$ → **1**, 0.$\overline{18}$*2 = 0.$\overline{36}$ → **0**, 0.$\overline{36}$*2 = 0.$\overline{72}$→ **0**, 0.$\overline{72}$*2=1.$\overline{45}$ → **1**, 0.$\overline{45}$*2 = 0.$\overline{90}$ → **0**, 0.$\overline{90}$*2= 1.$\overline{81}$ → **1**, 0.$\overline{81}$*2 = 1.$\overline{63}$ → **1**, 0.$\overline{63}$*2 = 1.$\overline{27}$ → **1**, 0.$\overline{27}$*2=0.$\overline{54}$ → **0**, 0.$\overline{54}$*2 = 1.$\overline{09}$ → **1**, 0.$\overline{09}$*2=0.$\overline{18}$ → **0**, ...e questo punto si ripete 0, 0, 1, 0, 1, 1, 1, 0, 1, 0 e cosi' via...

(notare che NON si deve mai troncare il numero: occorre mantenere tutte le cifre periodiche).

Dopo le prime 3 cifre binarie le cifre si ripetono (ribadendo la periodicita' del numero), quindi e'facilmente predicibile il resto delle 20 cifre binarie della mantissa. Inoltre la 24-esima cifra della mantissa corrisponde ad uno 0 quindi il piu'vicino numero rappresentabile in IEEE-754 singola precisione e'quello che si ottiene troncando cosi'com'e' il valore ottenuto per M. Quindi abbiamo ottenuto:

011 0010111010 0010111010 0010111010 ... ovvero M = 0110 0101 1101 0001 0111 010

Per l'esponente, ricordando che nel caso di singola precisione il valore della polarizzazione e' 127:

E = e+127 = 3+127=130 ovvero 1000 0010

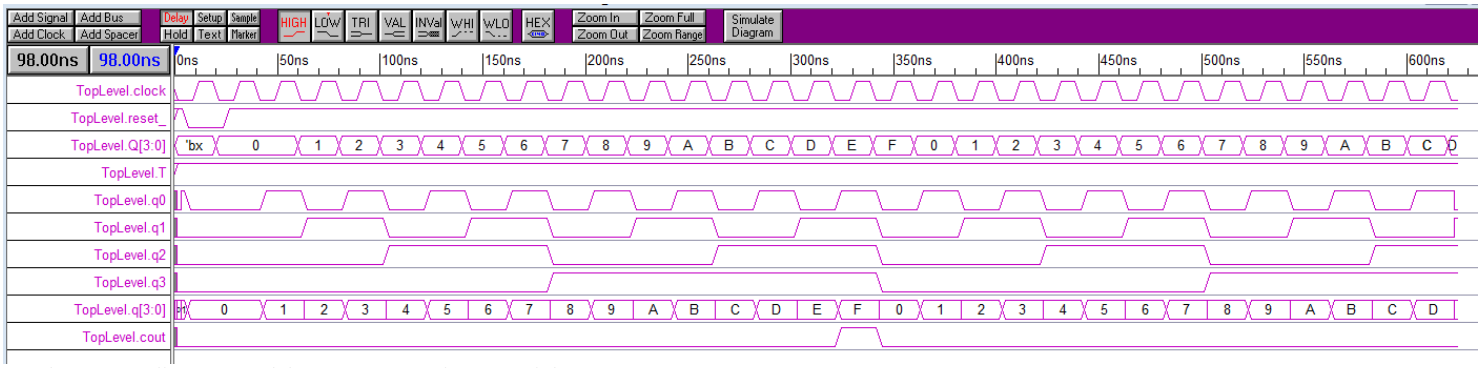
Inoltre per il segno S = 0

Quindi la rappresentazione cercata e':

0b 0100 0001 0011 0010 1110 1000 1011 1010

ESERCIZIO 4

```
`timescale 1ns/1ps
module TopLevel;
  reg clock; reg reset_;
  wire[3:0] Q;
  always #10 clock<=(!clock);
  initial begin
    $display ("time, \t clock, \t reset_, \t QQQQ");
    $monitor ("%g, \t %b, \t %b, \t %b", $time, clock, reset_,
Q);
    reset_ = 1'b1;
    clock = 0;
    #5 reset_ = 1'b0;
    #20 reset_ = 1'b1;
    #600 $finish;
  end
  reg T; initial begin T=1; #650 T=0; end
  Parallel_Carry_Counter prc(Q,T,clock,reset_);
  //debug:
  wire q0=prc.q0, q1=prc.q1, q2=prc.q2, q3=prc.q3;
  wire[3:0] q= {prc.q3,prc.q2,prc.q1,prc.q0};
  wire cout=prc.to3;
endmodule

// Flip-Flop T sensibile al fronte in discesa
// con riporto parallelo a 4-bit
module FFTnr(q,tin,c0,c1,c2,c3,tout,clock,reset_);
  input clock, reset_;
  input tin, c0, c1, c2, c3;
  output q,tout;
  reg STAR;
  parameter S0=0,S1=1;
  assign q=(STAR==S0)?0:1;
  assign #1 tout = c0 & c1 & c2 & c3 & q;
  always @(reset_==0) #1 STAR <= S0;
  always @(negedge clock) if (reset_==1) #3
    casex(STAR)
      S0: STAR <= (tin==0)?S0:S1;
      S1: STAR <= (tin==1)?S0:S1;
    endcase
endmodule

module Parallel_Carry_Counter(Q,T,clock,reset_);
  input clock, reset_,T;
  wire q0,q1,q2,q3,to0,to1,to2,to3;
  reg[3:0] Q1;
  output[3:0] Q; assign Q=Q1;
  FFTnr pc0(q0,  T, T,1'b1,1'b1, to0,clock,reset_);
  FFTnr pc1(q1,to0, T,  q0,1'b1,1'b1, to1,clock,reset_);
  FFTnr pc2(q2,to1, T,  q0,  q1,1'b1, to2,clock,reset_);
  FFTnr pc3(q3,to2, T,  q0,  q1,  q2, to3,clock,reset_);
  //notare che per non avere stati spuri in uscita conviene
bufferizzare in un registro
  always @(negedge clock) begin Q1[0]<=q0; Q1[1]<=q1; Q1[2]<=q2;
Q1[3]<=q3; end
endmodule
```



Confronto con diagramma del contatore con riporto seriale: