HIGH PERFORMANCE COMPUTER ARCHITECTURE midterm exam 28-06-2007 **MATRIC.NO.**_____

(former CALCOLATORI ELETTRONICI 2) **SURNAME**_____

FIRST NAME_____

1) (34/40) Consider the following snippet of code running on 4-ways out-of-order superscalar processor. Initially, R1=0x1000, R3=0x3000, R7=0x0003 and the other registers contain zero.

```
lab1:   LW   R2,0(R1)
        LW   R4,0(R3)
        ADD  R5,R5,R2
        ADD  R5,R5,R4
        MUL  R5,R5,R5
        SW   R5,0(R1)
        SW   R5,0(R3)
        ADDI R1,R1,4
        ADDI R3,R3,4
        ADDI R7,R7,-1
        BNE  R7,R0,lab1
```

Working hypothesis:
* the fetch, decode and commit stages are 4 instructions wide
* the instruction window has 16 slots
* we have 24 physical registers in the free pool
* the reorder buffer has unlimited size
* the integer multiplier has 4 stages
* the load/store queues have 3 slots each and a common effective-address calculation unit
* there are 4 ALUs for arithmetic and logic operations and for branching
* an ALU performs its operation in the same cycle when the operation is issued
* reads require 1 clock cycle (after the addressing phase)
* the register file has 4 input- and 4 output-ports
* there are 9 logical registers (including R0 which is hardwired to 0)
* the store operation leaves the issue stage as it is inserted in the store queue

In order to calculate the total cycles needed to execute 3 iterations of the above loop on such machine, complete the following chart until the end of the third iteration of the code fragment above, including the renamed stream the precise evolution of the free pool of the physical registers (the register map), the Instruction Window, the Reorder Buffer (ROB) and the Load Queue (LQ) and Store Queue (SQ).

Iter.	Instruction	F-Fetch (clock)	D-Decode (clock)	P-disPatch (clock)	I-Issue (clock)	X-eXecute (clock)	W-Write-back (clock)	C-Commit (clock)	Renamed Stream	Instruction Window Pi Pj Pk I Qj Qk	Reorder Buffer Ri Pi,old Cplt	Load Queue	Store Queue
1	**LW R2,0(R1)**	0							P2,0(P1)	P2 P1 - 0 0 0	R2 - -		
...	...												
...	...												

2) (6/40) Explain the difference between Processor Consistency and Weak Ordering by motivating the difference with a personal reasoning.

HIGH PERFORMANCE COMPUTER ARCHITECTURE midterm exam 28-06-2007

SOLUTION (REVISED 26/10/2018)

```
PHYSICAL REGS:  1  2  3  4  5  6  7  8  9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
                *           *  *  *                                       *  *
          qi:   0  1  1  1  0  0  0  1  1  1  1  1  1  1  1  1  1  1  1  1  0  0  1  1
          vi:  00 00 00 00 00 0C 0C 00 04 04 03 02 00 00 00 00 00 08 08 01 00 00 00 00

REG.FILE: Ri:          1         2         3         4         5         6         7         8
          Pi:          6        21         7        22         5         -         1         -
          Qi:          0         0         0         0         0         0         0         0
          Vi:  00001008 00000000 00003008 00000000 00000000 00000000 00000001 00000000

STAGES:                 F  D  P  I  X  W  C RENAMED-STR    INSTRUCTION-WINDOW                  REORDER-BUFFER           A  M  L  S  B  F  X
TOTAL SLOTS:            4  4 16  4 12  4  4 24             16                                  99                       4  1  1  0  1  4  1
BUSY SLOTS:             0  0  0  0  0  0  0 6              0                                   0                        0  0  0  0  0  0  0
STALLS:                 0  6  0104  0  0 13 6              0                                   0                        0  0  3 25  0  0  0

PC   INSTRUCTION        F  D  P  I  X  W  C Pi,Pj Pk Pl    IW#  OPCD Pi  Pj  Pk I/Pl  Cj Ck Cl  ROB# PC  Ri  oPi x s c  +--------------------+
000] LW   R2,0(R1)      0  1  2  3  4  6  7 P2,0(P1)       ----   LW P2  P1  -   0    2  -  -   ---- 000 R2  -   0 0 1  |LQ(0 )              |
001] LW   R4,0(R3)      0  1  2  4  5  7  8 P4,0(P3)       ----   LW P4  P3  -   0    2  -  -   ---- 001 R4  -   0 0 1  |PC   OP Pi  EFAD Ci|
002] ADD  R5,R5,R2      0  1  2  6  6  7  8 P6,P5,P2       ----  ADD P6  P5  P2  -    2  6  -   ---- 002 R5  P5  0 0 1  |---- LW P2  1000  6|
003] ADD  R5,R5,R4      0  1  2  7  7  8  9 P7,P6,P4       ----  ADD P7  P6  P4  -    7  7  -   ---- 003 R5  P6  0 0 1  |---- LW P4  3000  7|
004] MUL  R5,R5,R5      1  2  3  8  8 13 14 P8,P7,P7       ----  MUL P8  P7  P7  -    8  8  -   ---- 004 R5  P7  0 0 1  |---- LW P13 1004 10|
005] SW   R5,0(R1)      1  2  3  5  6 13 14 ,P0(P1)<-P8    ----   SW -   P8  P1  0    -  3  -   ---- 005 -   -   1 0 1  |---- LW P14 3004 11|
006] SW   R5,0(R3)      1  2  3  6  7 13 14 ,P0(P3)<-P8    ----   SW -   P8  P3  0    -  3  -   ---- 006 -   -   1 0 1  |---- LW P21 1008 13|
007] ADDI R1,R1,4       1  2  3  4  4  5 14 P9,P1,4        ---- ADDI P9  P1  -   4    3  -  -   ---- 007 R1  P1  0 0 1  |---- LW P22 3008 14|
008] ADDI R3,R3,4       2  3  4  5  5  6 15 P10,P3,4       ---- ADDI P10 P3  -   4    4  -  -   ---- 008 R3  P3  0 0 1  +--------------------+
009] ADDI R7,R7,-1      2  3  4  5  5  6 15 P12,P11,-1     ---- ADDI P12 P11 -   -1   4  -  -   ---- 009 R7  P11 0 0 1
010] BNE  R7,R0,-11     2  3  4  6  6  7 15 ,P12,P0,-11    ----  BNE -   P12 P0  -11  6  4  -   ---- 010 -   -   0 0 1  +--------------------+
011] LW   R2,0(R1)      3  4  5  7  8 10 15 P13,0(P9)      ----   LW P13 P9  -   0    5  -  -   ---- 000 R2  P2  0 0 1  |SQ(0 )              |
012] LW   R4,0(R3)      3  4  5  8  9 11 16 P14,0(P10)     ----   LW P14 P10 -   0    6  -  -   ---- 001 R4  P4  0 0 1  |PC   OP Pi  EFAD Ci|
013] ADD  R5,R5,R2      3  4  5 13 13 14 16 P15,P8,P13     ----  ADD P15 P8  P13 -   13 10  -   ---- 002 R5  P8  0 0 1  |---- SW P0  1000 13|
014] ADD  R5,R5,R4      3  4  5 14 14 15 16 P16,P15,P14    ----  ADD P16 P15 P14 -   14 11  -   ---- 003 R5  P15 0 0 1  |---- SW P0  3000 13|
015] MUL  R5,R5,R5      4  5  6 15 15 20 21 P17,P16,P16    ----  MUL P17 P16 P16 -   15 15  -   ---- 004 R5  P16 0 0 1  |---- SW P0  1004 20|
016] SW   R5,0(R1)      4  5  6  9 10 20 21 ,P0(P9)<-P17   ----   SW -   P17 P9  0    -  6  -   ---- 005 -   -   1 0 1  |---- SW P0  3004 20|
017] SW   R5,0(R3)      4  5  6 13 14 20 21 ,P0(P10)<-P17  ----   SW -   P17 P10 0    -  6  -   ---- 006 -   -   1 0 1  |---- SW P0  1008 27|
018] ADDI R1,R1,4       4  5  6  7  7  8 21 P18,P9,4       ---- ADDI P18 P9  -   4    6  -  -   ---- 007 R1  P9  0 0 1  |---- SW P0  3008 27|
019] ADDI R3,R3,4       5  6  7  8  8  9 22 P19,P10,4      ---- ADDI P19 P10 -   4    7  -  -   ---- 008 R3  P10 0 0 1  +--------------------+
020] ADDI R7,R7,-1      5  6  7  9  9 10 22 P20,P12,-1     ---- ADDI P20 P12 -   -1   7  -  -   ---- 009 R7  P12 0 0 1
021] BNE  R7,R0,-11     5  6  7  9  9 10 22 ,P20,P0,-11    ----  BNE -   P20 P0  -11  -  7  -   ---- 010 -   -   0 0 1
022] LW   R2,0(R1)      6  7  8 10 11 13 22 P21,0(P18)     ----   LW P21 P18 -   0    8  -  -   ---- 000 R2  P13 0 0 1
023] LW   R4,0(R3)      6  7  8 11 12 14 23 P22,0(P19)     ----   LW P22 P19 -   0    9  -  -   ---- 001 R4  P14 0 0 1
024] ADD  R5,R5,R2      6  7  8 20 20 21 23 P23,P17,P21    ----  ADD P23 P17 P21 -   20 13  -   ---- 002 R5  P17 0 0 1
025] ADD  R5,R5,R4      6  7  8 21 21 22 23 P24,P23,P22    ----  ADD P24 P23 P22 -   21 14  -   ---- 003 R5  P23 0 0 1
026] MUL  R5,R5,R5      7  8  9 22 22 27 28 P5,P24,P24     ----  MUL P5  P24 P24 -   22 22  -   ---- 004 R5  P24 0 0 1
027] SW   R5,0(R1)      7  8  9 14 15 27 28 ,P0(P18)<-P5   ----   SW -   P5  P18 0    -  9  -   ---- 005 -   -   1 0 1
028] SW   R5,0(R3)      7  8  9 20 21 27 28 ,P0(P19)<-P5   ----   SW -   P5  P19 0    -  9  -   ---- 006 -   -   1 0 1
029] ADDI R1,R1,4       7  9 10 11 11 12 28 P6,P18,4       ---- ADDI P6  P18 -   4    10 -  -   ---- 007 R1  P18 0 0 1
030] ADDI R3,R3,4       8 14 15 16 16 17 29 P7,P19,4       ---- ADDI P7  P19 -   4    15 -  -   ---- 008 R3  P19 0 0 1
031] ADDI R7,R7,-1      8 14 15 16 16 17 29 P1,P20,-1      ---- ADDI P1  P20 -   -1   15 -  -   ---- 009 R7  P20 0 0 1
032] BNE  R7,R0,-11     8 14 15 16 16 17 29 ,P1,P0,-11     ----  BNE -   P1  P0  -11  - 15  -   ---- 010 -   -   0 0 1
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