(POINTS 40/40) Snooping cache protocols can be write-invalidate or write-update. Both have drawbacks. A compromise is to have a mixed write-update/invalidate protocol. In this compromise protocol, called a competitive protocol, the basic protocol is update based. However, if a cache copy is updated more than once by a remote processor before a local access by the local processor, then the local copy is self-invalidated. To achieve this, we just need one bit associated with each cache block, call it the UP-bit. Whenever a cache block is loaded in cache, the UP-bit is set to 0. If an update is received for the block, the UP-bit is set to 1. Whenever an access is made locally by the processor attached to the cache, the UP-bit is set to 0. If an update is received by a cache block with the UP-bit equal to 1, then the block is invalidated locally. The protocol is a four-state, write-back protocol. The value returned by the bus shared line is represented by S in the state diagram; S0 is the shared state in which the UP-bit is 0, and S1 is the shared state in which the UP-bit is 1. States S0 and S1 are clean (memory is consistent because of the write through) and shared (multiple copies are possible). State D indicates a unique copy, which is possibly (but not necessarily) modified.

Draw the state diagram for this protocol. For each state transition, indicate the action that should be taken that is similar to the MSI protocols. Inputs to the finite state machine (FSM) are PrRd, PrWr, BusRd, and BusUpd. On some bus accesses there is a need to flush the block (explain why). Some transitions may end in two different states, depending on the value returned by the shared line.

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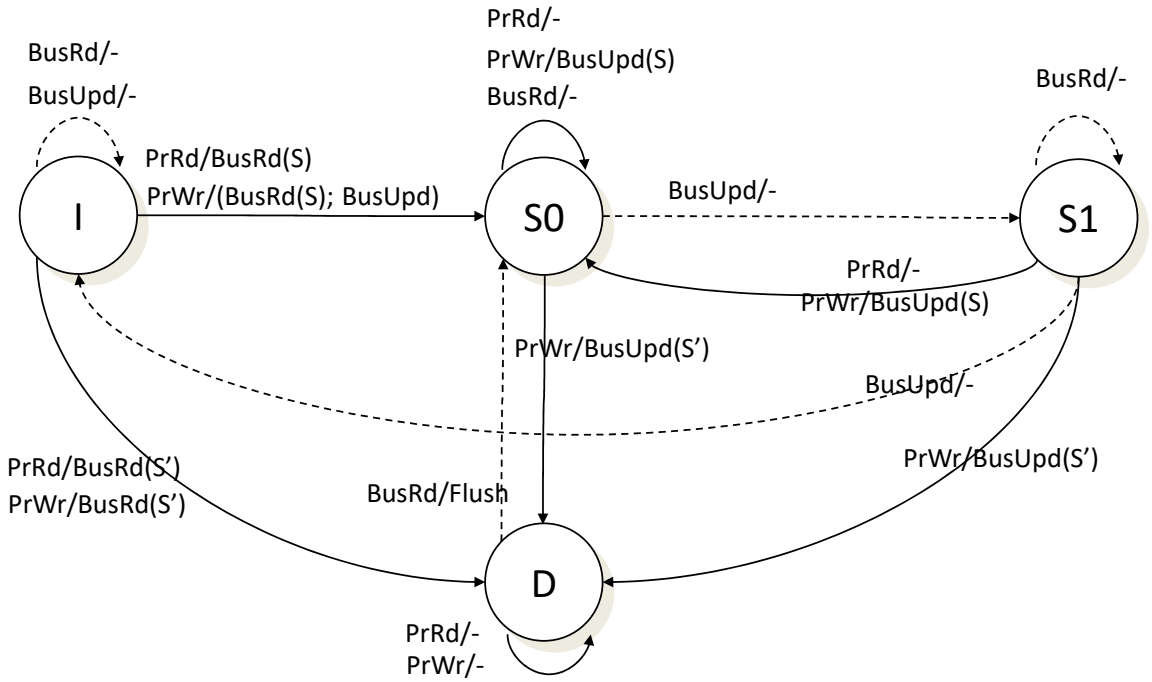
SOLUTION



- The Flush between D and S0 is necessary since S0 implies that the cache copy is updated with the memory while in the D state is not.
- The BusUpd is necessary after a PrWr (we may discover that the copy is a single one and then transition to D only after receiving the information from the Shared Line S).