HIGH PERFORMANCE COMPUTER ARCHITECTURE 30-06-2016 **MATRICOLATION NO.**_____

SURNAME_____

FIRST NAME_____

1) (POINTS 40/40) Consider the following snippet of code running on 4-ways out-of-order superscalar processor. Initially, R1=0x1000 and the other registers contain zero.

```
lab1:   LW   R2,0(R1)
        ADDI R2,R2,1
        MUL  R4,R2,R2
        SW   R4,0(R1)
        ADDI R1,R1,4
        BNE  R2,R0,lab1
```

Working hypothesis:
* the fetch, decode and commit stages are 4 instructions wide
* the instruction window has 8 slots
* we have 12 physical registers in the free pool
* the reorder buffer has unlimited size
* the integer multiplier has 4 stages
* the load/store queues have 3 slots each and a common effective-address calculation unit
* there are 4 ALUs for arithmetic and logic operations and for branching
* an ALU performs its operation in the same cycle when the operation is issued
* reads require 1 clock cycle (after the addressing phase)
* the register file has 4 input- and 4 output-ports
* there are 9 logical registers (including R0 which is hardwired to 0)
* the store operation leaves the issue stage as it is inserted in the store queue

In order to calculate the total cycles needed to execute 3 iterations of the above loop on such machine, complete the following chart until the end of the third iteration of the code fragment above, including the renamed stream the precise evolution of the free pool of the physical registers (the register map), the Instruction Window, the Reorder Buffer (ROB) and the Load Queue (LQ) and Store Queue (SQ).

EXERCIZE 1

```
PHYSICAL REGS:  1  2  3  4  5  6  7  8  9 10 11 12
                   *                       *  *
          qi:   1  0  1  1  1  1  1  1  1  1  0  0
          vi:  00 0C 01 01 04 00 01 01 08 00 01 01

REG.FILE: Ri:         1        2        3        4        5        6        7        8
          Pi:         2       11        -       12        -        -        -        -
          Qi:         0        0        0        0        0        0        0        0
          Vi:  00001008 00000000 00000000 00000001 00000000 00000000 00000000 00000000

STAGES:                F  D  P  I  X  W  C RENAMED-STR    INSTRUCTION-WINDOW                 REORDER-BUFFER          A  M  L  S  B  F  X
TOTAL SLOTS:           4  4  8  4 12  4  4 12             8                                  99                      4  1  1  0  1  4  1
BUSY SLOTS:            0  0  0  0  0  1  0 3              0                                  0                       0  0  0  0  0  0  0
STALLS:                0  2  0 25  0  0  5 2              0                                  0                       0  0  0  2  0  0  0

PC   INSTRUCTION       F  D  P  I  X  W  C Pi,Pj Pk Pl    IW#  OPCD Pi  Pj  Pk I/Pl  Cj Ck Cl  ROB# PC  Ri  oPi x s c  +--------------------+
000] LW   R2,0(R1)     0  1  2  3  4  6  7 P2,0(P1)       ----   LW P2  P1  -   0    2  -  -   ---- 000 R2  -   0 0 1  |LQ(0 )              |
001] ADDI R2,R2,1      0  1  2  6  6  7  8 P3,P2,1        ---- ADDI P3  P2  -   1    6  -  -   ---- 001 R2  P2  0 0 1  |PC   OP Pi  EFAD Ci|
002] MUL  R4,R2,R2     0  1  2  7  7 12 13 P4,P3,P3       ----  MUL P4  P3  P3  -    7  7  -   ---- 002 R4  -   0 0 1  |---- LW P2  1000  6|
003] SW   R4,0(R1)     0  1  2  4  5 12 13 ,P0(P1)<-P4    ----   SW -   P4  P1  0    -  2  -   ---- 003 -   -   1 0 1  |---- LW P6  1004  8|
004] ADDI R1,R1,4      1  2  3  4  4  5 13 P5,P1,4        ---- ADDI P5  P1  -   4    3  -  -   ---- 004 R1  P1  0 0 1  |---- LW P10 1008 10|
005] BNE  R2,R0,-6     1  2  3  4  4  5 13 ,P3,P0,-6      ----  BNE -   P3  P0  -6   -  3  -   ---- 005 -   -   0 0 1  +--------------------+
006] LW   R2,0(R1)     2  3  4  5  6  8 14 P6,0(P5)       ----   LW P6  P5  -   0    5  -  -   ---- 000 R2  P3  0 0 1
007] ADDI R2,R2,1      2  3  4  8  8  9 14 P7,P6,1        ---- ADDI P7  P6  -   1    8  -  -   ---- 001 R2  P6  0 0 1  +--------------------+
008] MUL  R4,R2,R2     2  3  4  9  9 14 15 P8,P7,P7       ----  MUL P8  P7  P7  -    9  9  -   ---- 002 R4  P4  0 0 1  |SQ(0 )              |
009] SW   R4,0(R1)     2  3  4  6  7 14 15 ,P0(P5)<-P8    ----   SW -   P8  P5  0    -  5  -   ---- 003 -   -   1 0 1  |PC   OP Pi  EFAD Cl|
010] ADDI R1,R1,4      3  4  5  6  6  7 15 P9,P5,4        ---- ADDI P9  P5  -   4    5  -  -   ---- 004 R1  P5  0 0 1  |---- SW P0  1000 12|
011] BNE  R2,R0,-6     3  4  5  7  7  8 15 ,P7,P0,-6      ----  BNE -   P7  P0  -6   -  5  -   ---- 005 -   -   0 0 1  |---- SW P0  1004 14|
012] LW   R2,0(R1)     4  5  6  7  8 10 16 P10,0(P9)      ----   LW P10 P9  -   0    7  -  -   ---- 000 R2  P7  0 0 1  |---- SW P0  1008 16|
013] ADDI R2,R2,1      4  5  6 10 10 11 16 P11,P10,1      ---- ADDI P11 P10 -   1   10  -  -   ---- 001 R2  P10 0 0 1  +--------------------+
014] MUL  R4,R2,R2     4  5  6 11 11 16 17 P12,P11,P11    ----  MUL P12 P11 P11 -   11 11  -   ---- 002 R4  P8  0 0 1
015] SW   R4,0(R1)     4  5  6  8  9 16 17 ,P0(P9)<-P12   ----   SW -   P12 P9  0    -  7  -   ---- 003 -   -   1 0 1
016] ADDI R1,R1,4      5  8  9 10 10 11 17 P2,P9,4        ---- ADDI P2  P9  -   4    9  -  -   ---- 004 R1  P9  0 0 1
017] BNE  R2,R0,-6     5  8  9 10 10 11 17 ,P11,P0,-6     ----  BNE -   P11 P0  -6   -  9  -   ---- 005 -   -   0 0 1
```

Therefore 18 cycles are needed for this configuration.