HIGH PERFORMANCE COMPUTER ARCHITECTURE midterm exam 29-10-2021 **MATR.NO.**_____

(MORE DETAILED FOR FUTURE REFERENCE) **SURNAME**_____

FIRST NAME_____

1) (POINTS 26/30) Consider the following snippet of code running on 4-ways out-of-order superscalar processor. Initially, R1=0x1000, R3=0x3000, R7=0x0003 and the other registers contain zero.

```
lab1:   LW   R2,0(R1)
        MUL  R4,R2,R2
        SW   R4,0(R1)
        ADDI R1,R1,4
        BNE  R2,R0,lab1
```

Working hypothesis:

- the fetch, decode and commit stages are 4 instructions wide
- **the instruction window has 10 slots**
- **we have 10 physical registers in the free pool (excluding P0 which is hardwired to 0)**
- **the reorder buffer has 10 entries**
- the integer multiplier has 4 stages
- the load/store queues have 3 slots each and a common effective-address calculation unit
- there is 1 ALUs for arithmetic and logic operations and 1 ALU for branching
- an ALU/BRANCH performs its operation in the same cycle when the operation is issued
- reads require 1 clock cycle (after the addressing phase)
- the register file has 4 input- and 4 output-ports
- there are 8 logical registers (excluding R0 which is hardwired to 0)
- the store operation leaves the issue stage as it is inserted in the store queue
- when the X stage finds a free slot in the LQ/SQ, also a slot in the I stage is reserved
- branches are predicted taken

Calculate the total cycles, needed to execute 3 iterations of the above loop on such machine, complete the following chart until the end of the third iteration of the code fragment above, including the renamed stream the precise evolution of the free pool of the physical registers (the register map), the Instruction Window, the Reorder Buffer (ROB) and the Load Queue (LQ) and Store Queue (SQ).
Note: Ci, Cj, Ck, Cl indicate the cycle when the corresponding physical registers are available in IW.

Iter.	Instruction	F Fetch (clock)	D Decode (clock)	P disPatch (clock)	I Issue (clock)	X eXecute (clock)	W Wr.back (clock)	C Commit (clock)	Renamed Stream	Instruction Window Pi Pj Pk I/Pl Ci Cj Ck Cl	Reorder Buffer Ri Pi,old Cplt	Load Queue PC Pi Ci	Store Queue PC Pj Cj
1	**LW R2,0(R1)**	0							P2,0(P1)	P2 P1 - 0 0 0 0 -	R2 - -		
…	…												
…	…												

2) (POINTS 4/30) Write a single command pipe for Linux to find all files whose name that starts with ‘result’ followed by two numeric digits and store them in the file ‘mio’.

HIGH PERFORMANCE COMPUTER ARCHITECTURE midterm exam 29-10-2021 - SOLUTION

1) It takes 20 cycles, in fact:

```
================================================================================================================================================================
PHYSICAL REGS:  1  2  3  4  5  6  7  8  9 10
                                       *  *  *
          qi:   1  1  1  1  1  1  1  0  0  0
          vi:  00 00 00 04 00 00 08 00 00 0C
================================================================================================================================================================
REG.FILE: Ri:         1        2        3        4        5        6        7        8
          Pi:        10        8        -        9        -        -        -        -
          Qi:         0        0        0        0        0        0        0        0
          Vi:  00001008 00000000 00003000 00000000 00000000 00000000 00000003 00000000
================================================================================================================================================================
STAGES:                 F  D  P  I  X  W  C RENAMED-STR    INSTRUCTION-WINDOW                 REORDER-BUFFER           A  M  L  S  B  F  X
TOTAL SLOTS:            4  4 10  4 12  4  4 10             10                                 10                       4  1  1  0  1  4  1
BUSY SLOTS:             0  0  0  0  0  1  0 3              0                                  0                        0  0  0  0  0  0  0
STALLS:                 0  1  6  8  0  0  9 0              0                                  6                        0  0  0  2  0  0  0
================================================================================================================================================================
PC   INSTRUCTION        F  D  P  I  X  W  C Pi,Pj Pk Pl    IW#  OPCD Pi  Pj  Pk I/Pl  Cj Ck Cl  ROB# PC  Ri  oPi s x c  +--------------------+
000] LW   R2,0(R1)      0  1  2  3  4  6  7 P2,0(P1)      ----   LW P2  P1  -   0    2  -  -   ---- 000 R2  -   0 0 1  |LQ(0 )              |
001] MUL  R4,R2,R2      0  1  2  6  6 11 12 P3,P2,P2       ----  MUL P3  P2  P2  -    6  6  -   ---- 001 R4  -   0 0 1  |PC   OP Pi  EFAD Ci|
002] SW   R4,0(R1)      0  1  2  4  5 11 12 ,0(P1)<-P3     ----   SW -   P3  P1  0    -  2  -   ---- 002 -   -   1 0 1  |---- LW P2  1000  6|
003] ADDI R1,R1,4       0  1  2  3  3  4 12 P4,P1,4        ---- ADDI P4  P1  -   4    2  -  -   ---- 003 R1  P1  0 0 1  |---- LW P5  1004  8|
004] BNE  R2,R0,-5      1  2  3  4  4  5 12 ,P2,P0,-5      ----  BNE -   P2  P0  -5   -  3  -   ---- 004 -   -   0 0 1  |---- LW P8  1008 11|
005] LW   R2,0(R1)      2  3  4  5  6  8 13 P5,0(P4)       ----   LW P5  P4  -   0    4  -  -   ---- 000 R2  P2  0 0 1  +--------------------+
006] MUL  R4,R2,R2      2  3  4  8  8 13 14 P6,P5,P5       ----  MUL P6  P5  P5  -    8  8  -   ---- 001 R4  P3  0 0 1
007] SW   R4,0(R1)      2  3  4  6  7 13 14 ,0(P4)<-P6     ----   SW -   P6  P4  0    -  4  -   ---- 002 -   -   1 0 1  +--------------------+
008] ADDI R1,R1,4       2  3  4  5  5  6 14 P7,P4,4        ---- ADDI P7  P4  -   4    4  -  -   ---- 003 R1  P4  0 0 1  |SQ(0 )              |
009] BNE  R2,R0,-5      3  4  5  6  6  7 14 ,P5,P0,-5      ----  BNE -   P5  P0  -5   -  5  -   ---- 004 -   -   0 0 1  |PC   OP Pj  EFAD Cj|
010] LW   R2,0(R1)      4  5  7  8  9 11 15 P8,0(P7)       ----   LW P8  P7  -   0    7  -  -   ---- 000 R2  P5  0 0 1  |---- SW P3  1000 11|
011] MUL  R4,R2,R2      4  5 12 13 13 18 19 P9,P8,P8       ----  MUL P9  P8  P8  -   12 12  -   ---- 001 R4  P6  0 0 1  |---- SW P6  1004 13|
012] SW   R4,0(R1)      4  5 12 13 14 18 19 ,0(P7)<-P9     ----   SW -   P9  P7  0    - 12  -   ---- 002 -   -   1 0 1  |---- SW P9  1008 18|
013] ADDI R1,R1,4       4  5 12 13 13 14 19 P10,P7,4       ---- ADDI P10 P7  -   4   12  -  -   ---- 003 R1  P7  0 0 1  +--------------------+
014] BNE  R2,R0,-5      5  7 12 13 13 14 19 ,P8,P0,-5      ----  BNE -   P8  P0  -5   - 12  -   ---- 004 -   -   0 0 1
```

2) `find . -name "^result[0-9][0-9]" > mio`