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SURNAME \_\_\_\_\_

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Consider a bus-based multicore that supports a new cache-coherence protocol called MOESI. Compared to the well-known MESI protocol, the MOESI protocol adds a 5<sup>th</sup> state called O (Owned). A copy in O state is like a SM copy in Dragon: the owned copy is modified and the “owner cache” has the responsibility to provide the copy once a BusRd transaction involves that copy; at the same time, the M state is now simplified, as it doesn’t have to update memory on Flush (only Flush\* transactions appear in this protocol). A copy enters the O state if another cache needs a copy (for reading) while that copy is in M state; on a local read, local write or other bus transactions, the O copy behaves like an S copy.

1a) [Points 8/30] Draw the diagram of the MESIF protocol according to the above description.



1b) [ Points 22/30] Assuming a cost of 1cc (1 clock-cycle) for read/write operations, 90cc for BusRd or BusRdx transactions, 60cc for BusUpgr, 20 cc for Flush\* and 30cc for Flush. Evaluate the total cost (in clock-cycles) for the following streams:

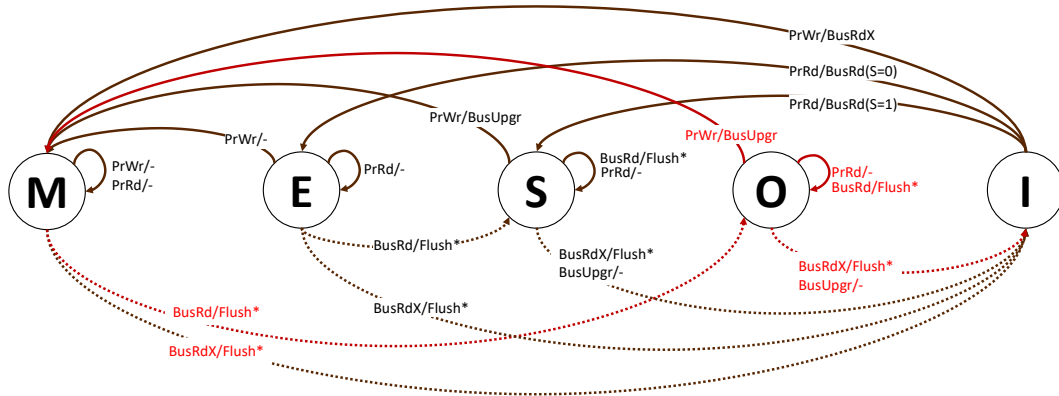
<b>stream-1 MOESI</b>	<b>Core Operation</b>	<b>C1</b>	<b>C2</b>	<b>C3</b>	<b>Bus Transaction</b>	<b>Data from</b>	<b>Cycles</b>	
	PrRd1							
	PrWr1							
	PrRd1							
	PrWr1							
	PrRd2							
	PrWr2							
	PrRd2							
	PrWr2							
	PrRd3							
	PrWr3							
	PrRd3							
	PrWr3							
<b>TOTAL</b>								
<b>stream-2 MOESI</b>	<b>Core Operation</b>	<b>C1</b>	<b>C2</b>	<b>C3</b>	<b>Bus Transaction</b>	<b>Data from</b>	<b>Cycles</b>	
	PrRd1							
	PrRd2							
	PrRd3							
	PrWr1							
	PrWr2							
	PrWr3							
	PrRd1							
	PrRd2							
	PrRd3							
	PrWr3							
	PrWr1							
	<b>TOTAL</b>							
<b>stream-3 MOESI</b>	<b>Core Operation</b>	<b>C1</b>	<b>C2</b>	<b>C3</b>	<b>Bus Transaction</b>	<b>Data from</b>	<b>Cycles</b>	
	PrRd1							
	PrRd2							
	PrRd3							
	PrRd3							
	PrWr1							
	PrWr1							
	PrWr1							
	PrWr1							
	PrWr2							
	PrWr3							
	<b>TOTAL</b>							

**EXERCISE 1a)**

First, we start drawing the states of the MESI protocol, and then let's focus on the M-state and O-state.

**M-state:** PrRd and PrWr are exactly as in MESI; however, when there is a BusRd, the copy enters into O-state while providing the copy to the requesting cache (via a Flush\* transactions) without the need of updating the memory; since it is now the cache with the copy in O-state that has the responsibility to provide a shared-modified copy, the memory is updated on replacement (i.e., for cache conflicts) of M copies or O copies. If a BusRdX transaction is observed in M-state, that cache provides the copy (via a Flush\* transaction ) to the requesting cache and change its state from M to I.

**O-state:** since it is now this state that has the responsibility to update memory on replacement or to provide the copy to other caches, the local read or write behave like in the S-state; similar for BusRd, BusRdX or BusUpgr the O-state will have the same behavior for operations and transactions happening in the S-state.



**EXERCISE 1b)**

stream-1 MOESI	Core Operation	C1	C2	C3	Bus Transaction	Data from	Cycles
	PrRd1	E	I	I	BusRd (S=0)	Mem	90
PrWr1	M			-	-	1	
PrRd1	M			-	-	1	
PrWr1	M			-	-	1	
PrRd2	O	S		BusRd (S=1) , Flush*	C1	90+20	
PrWr2	I	M		BusUpgr	-	60	
PrRd2		M		-	-	1	
PrWr2		M		-	-	1	
PrRd3		O	S	BusRd (S=1) , Flush*	C2	90+20	
PrWr3		I	M	BusUpgr	-	60	
PrRd3			M	-	-	1	
PrWr3			M	-	-	1	
<b>TOTAL</b>							<b>437</b>

stream-2 MOESI	Core Operation	C1	C2	C3	Bus Transaction	Data from	Cycles
	PrRd1	E	I	I	BusRd (S=0)	Mem	90
PrRd2	S	S		BusRd (S=1) , Flush*	C1	90+20	
PrRd3	S	S	S	BusRd (S=1) , Flush*	C1/C2	90+20	
PrWr1	M	I	I	BusUpgr	-	60	
PrWr2	I	M		BusRdX, Flush*	C1	90+20	
PrWr3		I	M	BusRdX, Flush*	C2	90+20	
PrRd1	S		O	BusRd (S=1) , Flush*	C3	90+20	
PrRd2	S	S	O	BusRd (S=1) , Flush*	C3	90+20	
PrRd3	S	S	O	-	-	1	
PrWr3	I	I	M	BusUpgr	-	60	
PrWr1	M		I	BusRdX, Flush*	C3	90+20	
<b>TOTAL</b>							<b>981</b>

stream-3 MOESI	Core Operation	C1	C2	C3	Bus Transaction	Data from	Cycles
	PrRd1	E	I	I	BusRd (S=0)	Mem	90
PrRd2	S	S		BusRd (S=1) , Flush*	C1	90+20	
PrRd3	S	S	S	BusRd (S=1) , Flush*	C1/C2	90+20	
PrRd3	S	S	S	-	-	1	
PrWr1	M	I	I	BusUpgr	-	60	
PrWr1	M			-	-	1	
PrWr1	M			-	-	1	
PrWr1	M			-	-	1	
PrWr2	I	M		BusRdX, Flush*	C1	90+20	
PrWr3		I	M	BusRdX, Flush*	C2	90+20	
<b>TOTAL</b>							<b>594</b>